



## HNS P-Channel Enhancement Mode Power MOSFET

### Description

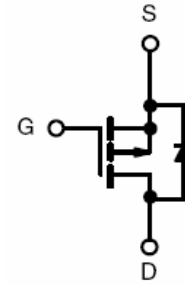
The HNS60D12K uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. This device is well suited for high current load applications.

### General Features

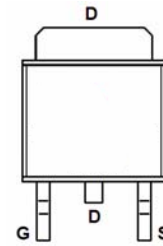
- $V_{DS} = -60V, I_D = -12A$   
 $R_{DS(ON)} < 100m\Omega @ V_{GS} = -10V$   
 $R_{DS(ON)} < 125m\Omega @ V_{GS} = -4.5V$
- High density cell design for ultra low  $R_{DS(on)}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high  $E_{AS}$
- Excellent package for good heat dissipation

### Application

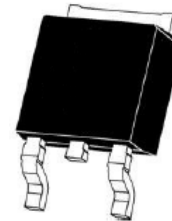
- High side switch for full bridge converter
- DC/DC converter for LCD display



Schematic diagram



pin assignment



TO-252 -2Ltop view

### Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
HNS60D12K	HNS60D12K	TO-252-2L	-	-	-

### Absolute Maximum Ratings ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	-60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	-12	A
Drain Current-Continuous( $T_C = 100^\circ\text{C}$ )	$I_D(100^\circ\text{C})$	-8.5	A
Pulsed Drain Current	$I_{DM}$	-30	A
Maximum Power Dissipation	$P_D$	60	W
Derating factor		0.4	W/ $^\circ\text{C}$
Single pulse avalanche energy <sup>(Note 5)</sup>	$E_{AS}$	50	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 175	$^\circ\text{C}$

### Thermal Characteristic

Thermal Resistance, Junction-to-Case <sup>(Note 2)</sup>	$R_{\theta JC}$	2.5	$^\circ\text{C/W}$
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**Electrical Characteristics ( $T_C=25^{\circ}\text{C}$  unless otherwise noted)**

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V I <sub>D</sub> =-250μA	-60	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-60V, V <sub>GS</sub> =0V	-	-	-1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±100	nA
On Characteristics <sup>(Note 3)</sup>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250μA	-1	-1.5	-2.2	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =-10V, I <sub>D</sub> =-12A	-	84	100	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-8A	-	100	125	mΩ
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =-5V, I <sub>D</sub> =-12A	-	10	-	S
Dynamic Characteristics <sup>(Note4)</sup>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =-30V, V <sub>GS</sub> =0V, F=1.0MHz	-	1630.7	-	PF
Output Capacitance	C <sub>oss</sub>		-	90.6	-	PF
Reverse Transfer Capacitance	C <sub>rss</sub>		-	77.3	-	PF
Switching Characteristics <sup>(Note 4)</sup>						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =-30V, R <sub>L</sub> =1.5Ω, V <sub>GS</sub> =-10V, R <sub>G</sub> =3Ω	-	11	-	nS
Turn-on Rise Time	t <sub>r</sub>		-	14	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	33	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	13	-	nS
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =-30, I <sub>D</sub> =-12A, V <sub>GS</sub> =-10V	-	37.6		nC
Gate-Source Charge	Q <sub>gs</sub>		-	4.3		nC
Gate-Drain Charge	Q <sub>gd</sub>		-	7.2		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage <sup>(Note 3)</sup>	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =-12A	-		-1.2	V
Diode Forward Current <sup>(Note 2)</sup>	I <sub>S</sub>		-	-	-12	A
Reverse Recovery Time	t <sub>rr</sub>	TJ = 25°C, IF =- 12A	-	35		nS
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = -100A/μs <sup>(Note3)</sup>	-	38		nC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

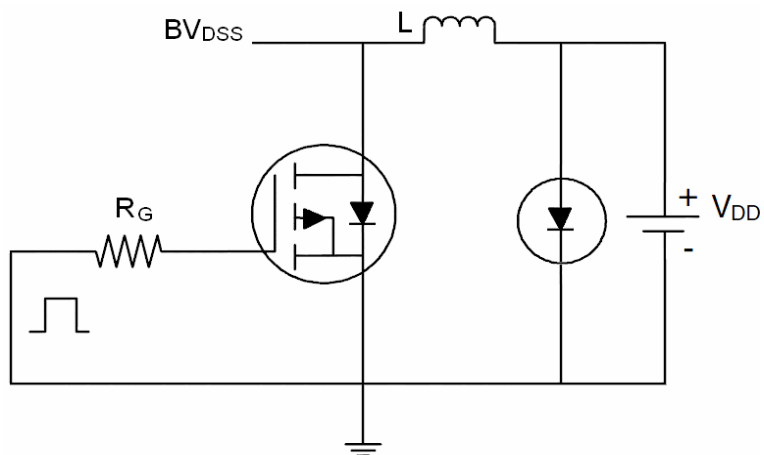
**Notes:**

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production
5.  $E_{AS}$  condition:  $T_J=25^{\circ}\text{C}, V_{DD}=-20V, V_G=-10V, L=1mH, R_G=25\Omega$

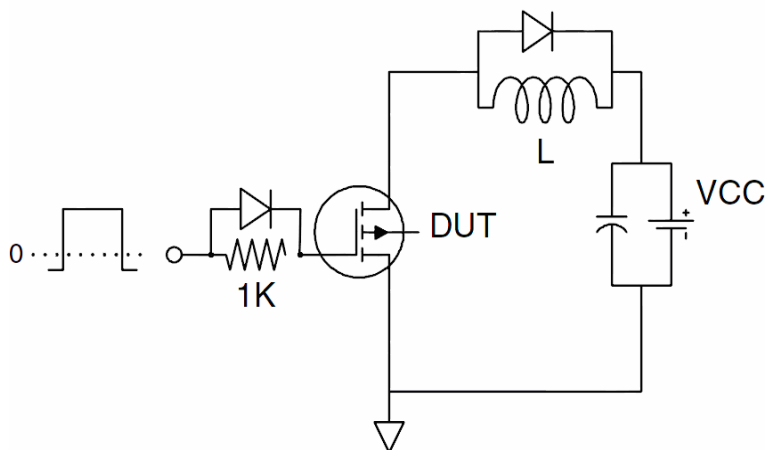


## Test Circuit

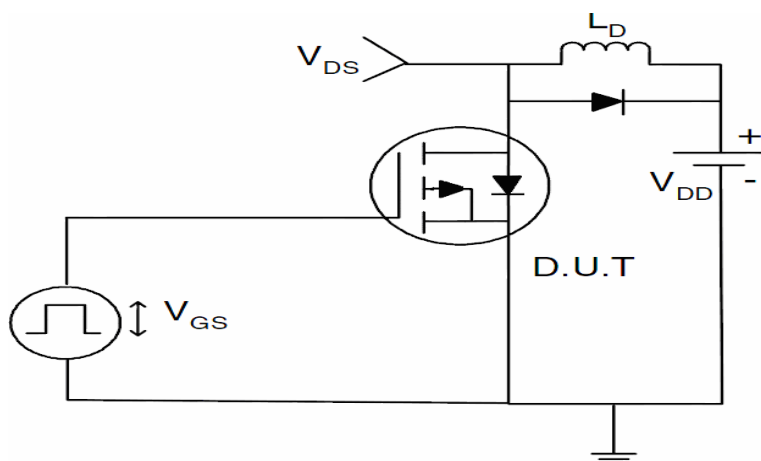
### 1) $E_{AS}$ Test Circuit



### 2) Gate Charge Test Circuit



### 3) Switch Time Test Circuit





## Typical Electrical and Thermal Characteristics (Curves)

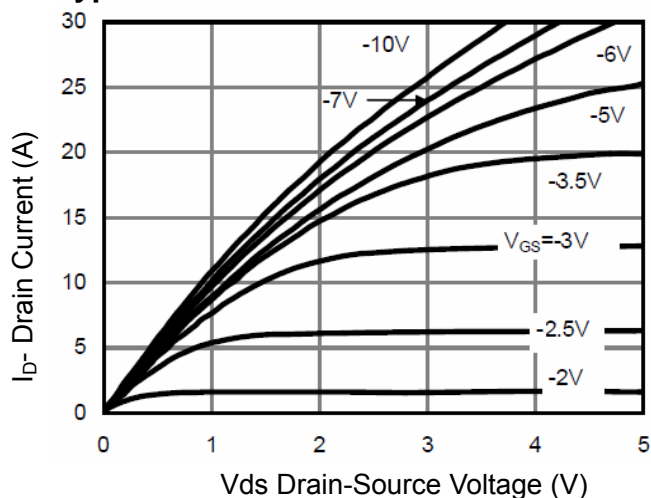


Figure 1 Output Characteristics

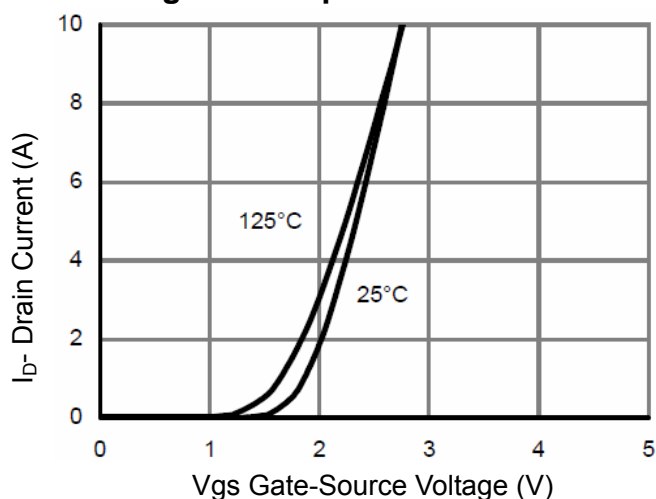


Figure 2 Transfer Characteristics

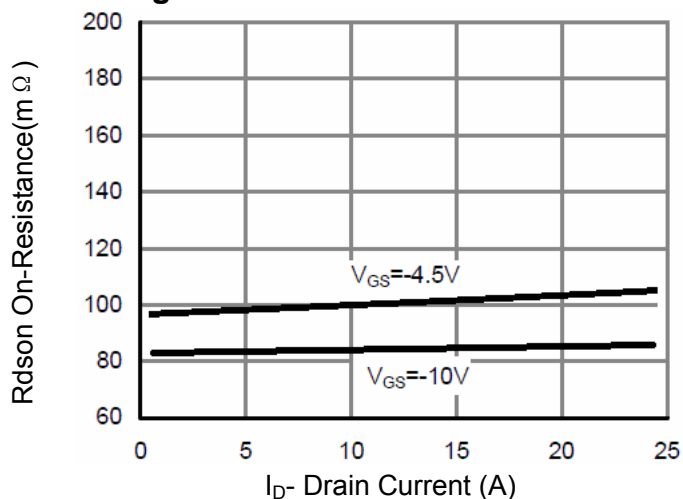


Figure 3  $R_{DS(on)}$ - Drain Current

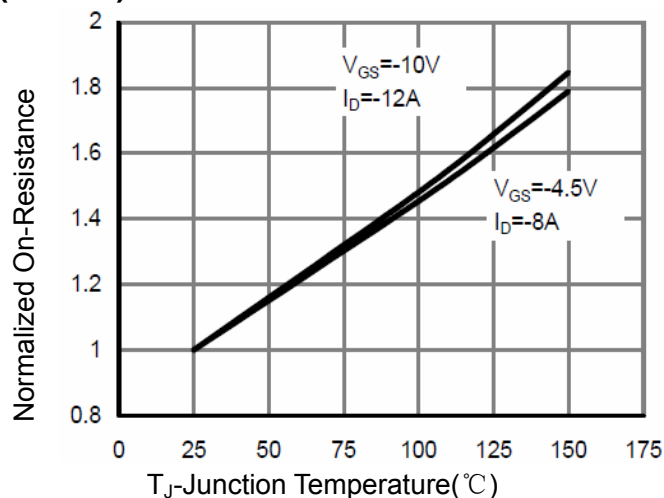


Figure 4  $R_{DS(on)}$ -Junction Temperature

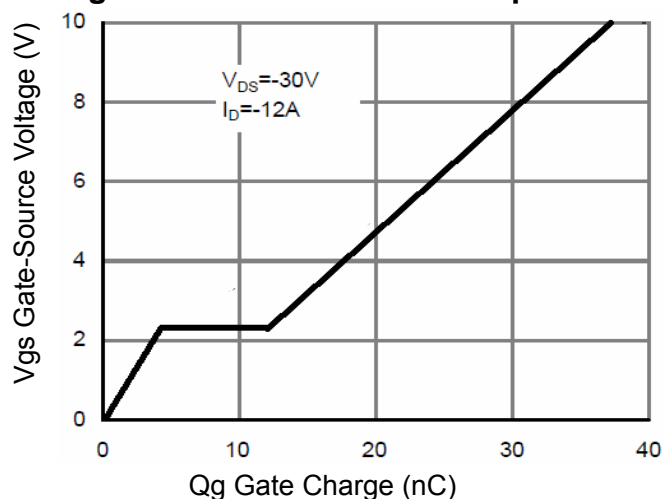


Figure 5 Gate Charge

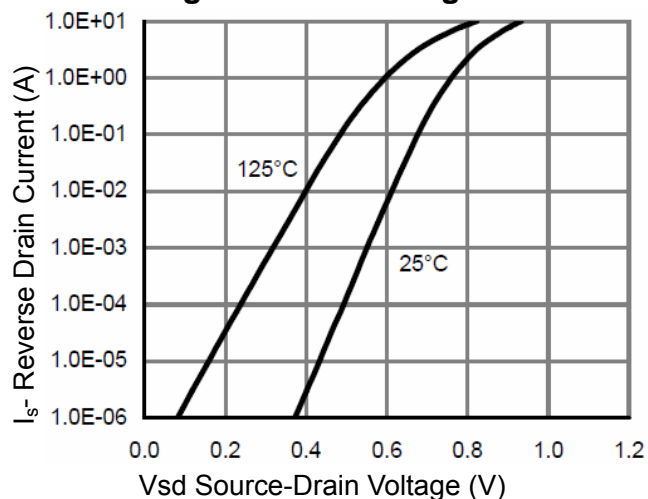


Figure 6 Source- Drain Diode Forward

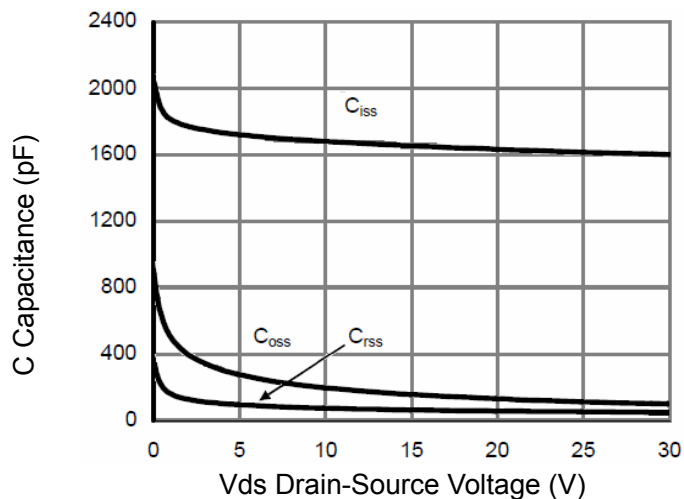


Figure 7 Capacitance vs Vds

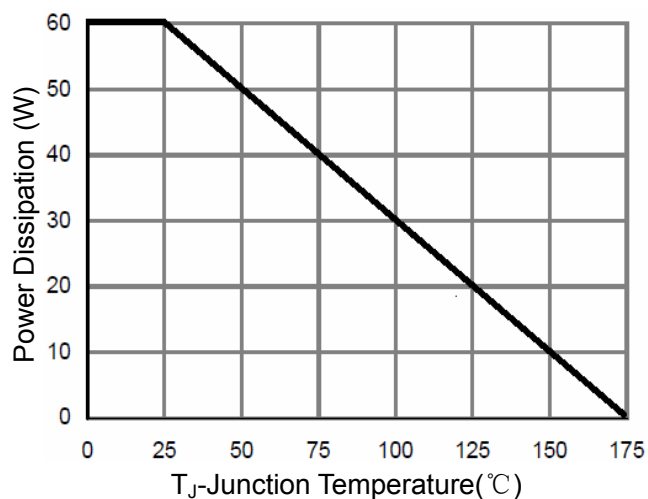


Figure 9 Power De-rating

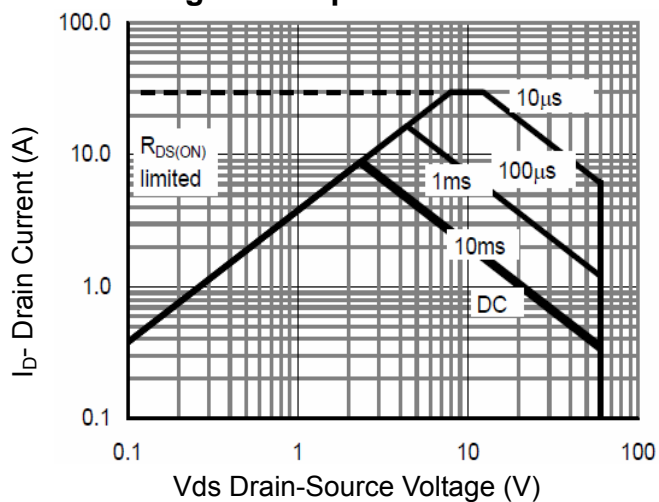


Figure 8 Safe Operation Area

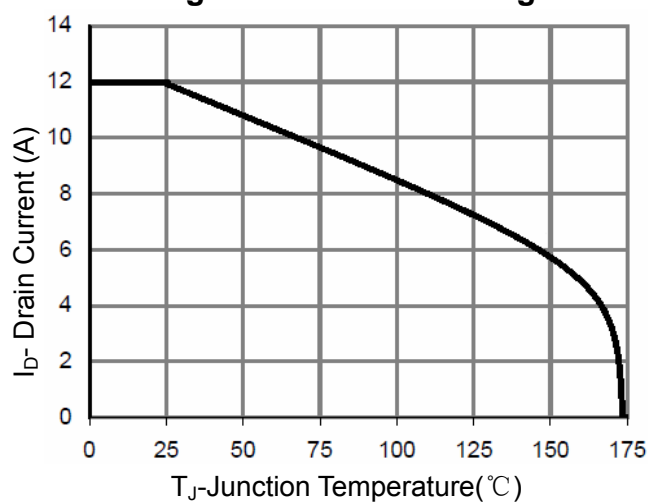


Figure 10 ID Current De-rating

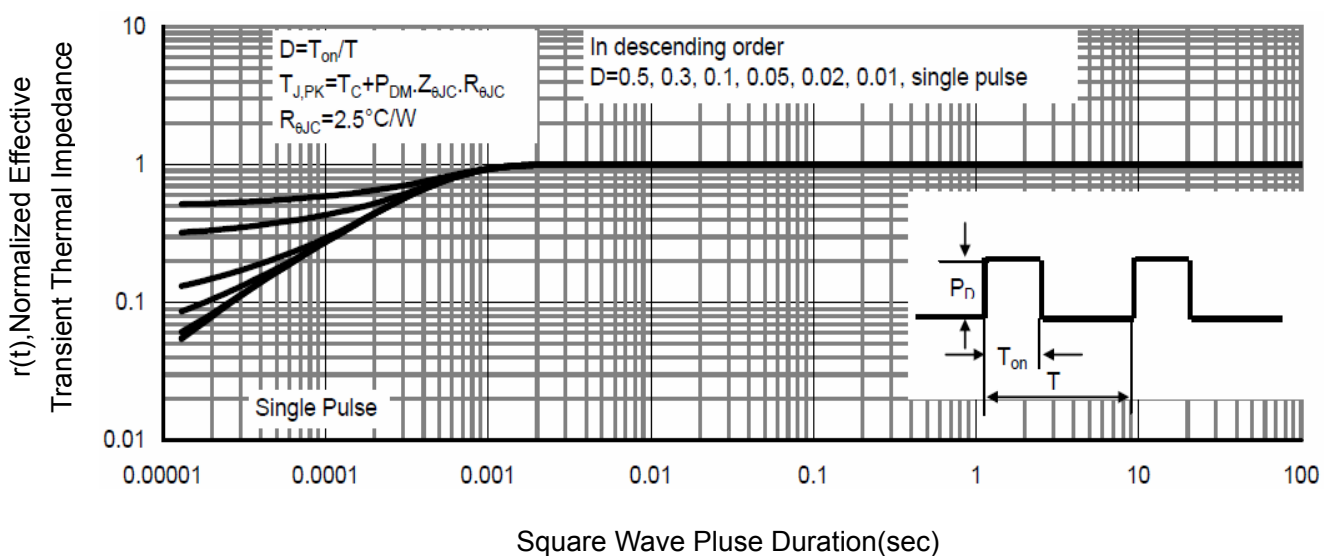
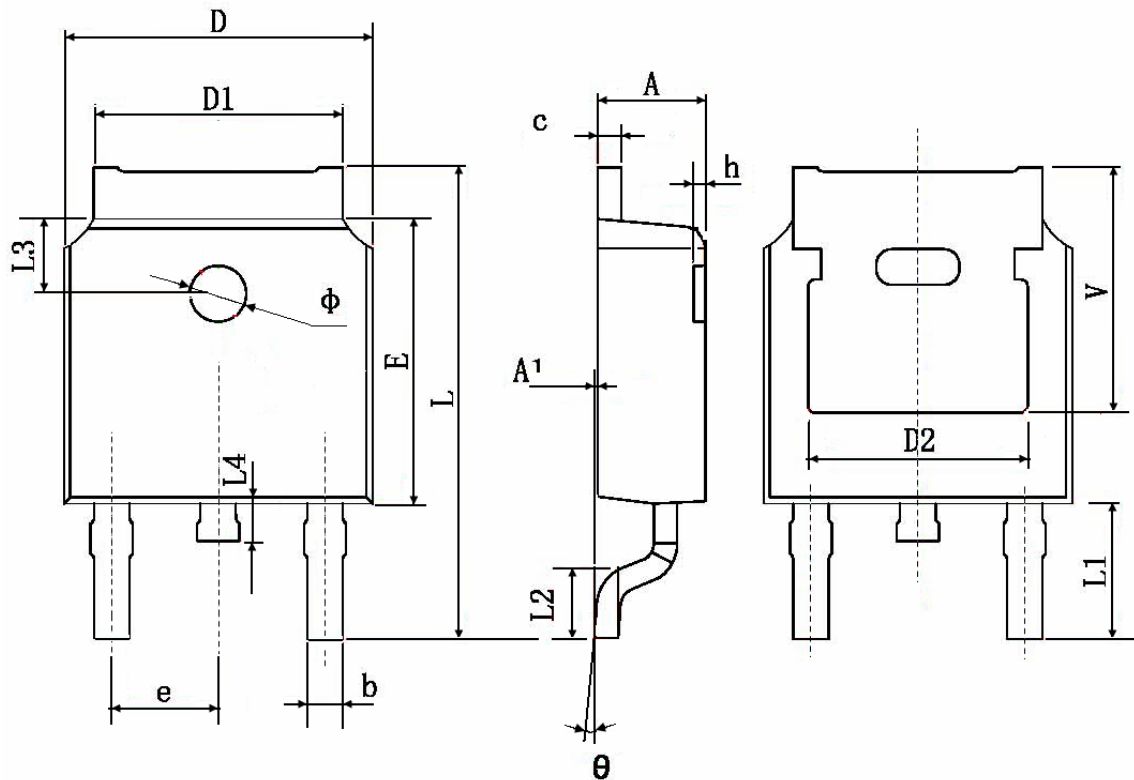


Figure 11 Normalized Maximum Transient Thermal Impedance



TO-252 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	

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