

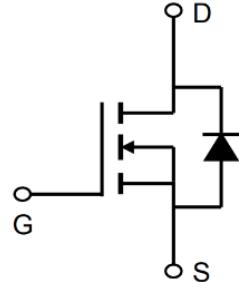
## 200V N-Channel Enhancement Mode MOSFET

### Description

The HN70N20MP is silicon N-channel Enhanced

VDMOSFETs, is obtained by the self-aligned planar Technology

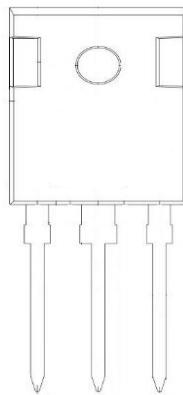
which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.



### General Features

VDS =200V, ID =70A

RDS(ON) <38mΩ@ VGS=10V



### Application

Power amplifier

motor drive

### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
HN70N20MP	TO-247-3 Plus	HN70N20MP XXX YYYY	600
HN70N20MP	TO-247-3L	HN70N20MP XXX YYYY	600

**Absolute Maximum Ratings**  $T_c = 25^\circ\text{C}$ , unless otherwise noted

Symbol	Parameter	Rating	Units
VDSS	Drain-to-Source Voltage	200	V
ID	Continuous Drain Current $T_c = 25^\circ\text{C}$	70	A
	Continuous Drain Current $T_c = 100^\circ\text{C}$	42	A
IDMa1	Pulsed Drain Current $T_c = 25^\circ\text{C}$	280	A
VGS	Gate-to-Source Voltage	$\pm 30$	V
EAS a2	Single Pulse Avalanche Energy	2200	mJ
PD	Power Dissipation $T_c = 25^\circ\text{C}$	367	W
	Derating Factor above $25^\circ\text{C}$	2.9	W/ $^\circ\text{C}$
TJ, Tstg	Operating Junction and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
TL	Maximum Temperature for Soldering	300	$^\circ\text{C}$
R <sub>θJC</sub>	Junction-to-Case	0.34	$^\circ\text{C}/\text{W}$
R <sub>θJA</sub>	Junction-to-Ambient	40	$^\circ\text{C}/\text{W}$

## 200V N-Channel Enhancement Mode MOSFET

**Electrical Characteristics** at  $T_j=25\text{ }^\circ\text{C}$  unless otherwise specified

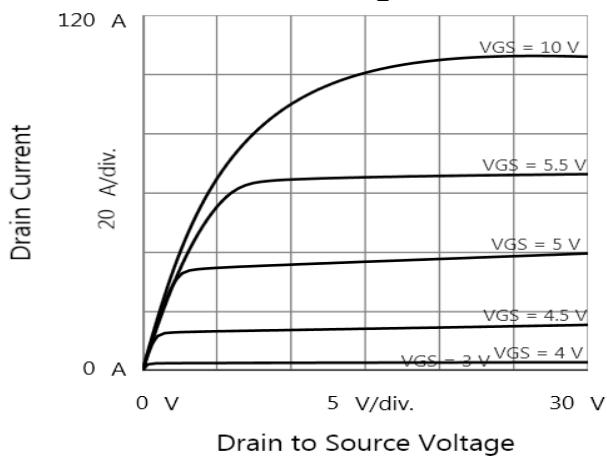
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V(BR)DSS	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}, I_D=250\mu\text{A}$	200	--	--	V
IDSS	Zero Gate Voltage Drain Current	$V_{DS}=200\text{V}, V_{GS}=0\text{V}, T_j=25\text{ }^\circ\text{C}$	--	--	1	$\mu\text{A}$
IGSS	Gate-Source Leakage	$V_{GS}=\pm 20\text{V}, V_{DS}=0\text{V}$	--	--	$\pm 100$	nA
VGS(th)	Gate-Source Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	2	--	4	V
RDS(on)	Drain-Source On-Resistance (Note4)	$V_{GS}=10\text{V}, I_D=25\text{A}$	--	30	38	$\text{m}\Omega$
$C_{iss}$	Input Capacitance	$V_{GS}=0\text{V}, V_{DS}=25\text{V}, f=1.0\text{MHz}$	--	3538	--	pF
$C_{oss}$	Output Capacitance		--	657	--	
$C_{rss}$	Reverse Transfer Capacitance		--	280	--	
$Q_g$	Total Gate Charge	$V_{DD}=160\text{V}, I_D=50\text{A}, V_{GS}$ 0 to 10V	--	244	--	nC
$Q_{gs}$	Gate-Source Charge		--	16	--	
$Q_{gd}$	Gate-Drain Charge		--	144	--	
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=100\text{V}, I_D=50\text{A}, V_{GS}=10\text{V}, R_G=25\Omega$	--	53	--	ns
$t_r$	Turn-on Rise Time		--	65	--	
$t_{d(off)}$	Turn-off Delay Time		--	689	--	
$t_f$	Turn-off Fall Time		--	230	--	
ISD	Continuous Source Current	Integral PN-diode in MOSFET	--	--	50	A
ISM	Pulsed Source Current		--	--	200	
$V_{SD}$	Body Forward Voltage	$I_S=20\text{A}, V_{GS}=0\text{V}$	--	--	1.5	V
trr	Reverse Recovery Time	$V_{GS}=0\text{V}, I_F=10\text{A}, di_F/dt=100\text{A}/\mu\text{s}$	--	208	--	ns
Qrr	Reverse Recovery Charge		--	2.04	--	$\mu\text{C}$

1、Repetitive Rating: Pulse width limited by maximum junction temperature

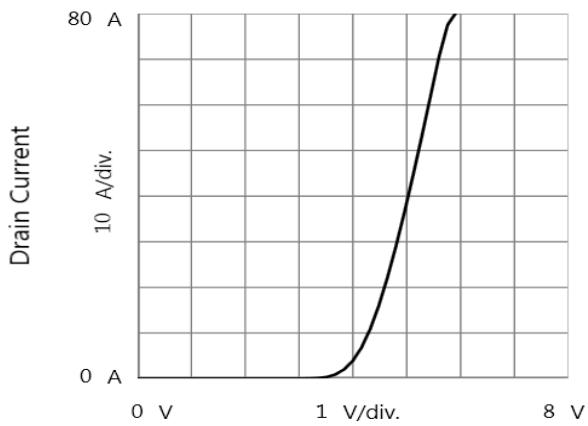
2、 $L=1\text{mH}, V_{DD}=30\text{V}, R_G=25\Omega$ , Starting  $T_j=25\text{ }^\circ\text{C}$  3. Pulse Test: Pulse width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 1\%$

## 200V N-Channel Enhancement Mode MOSFET

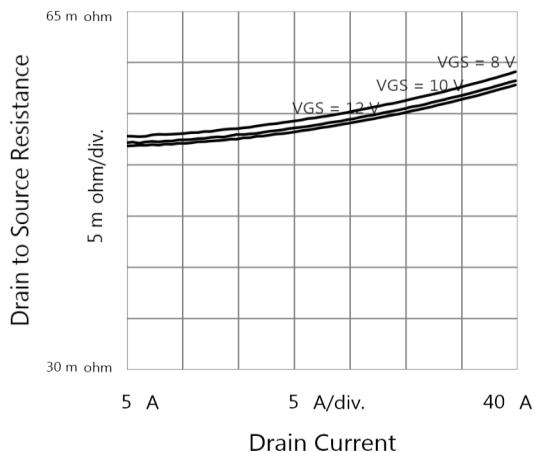
### Electrical Characteristics Diagrams



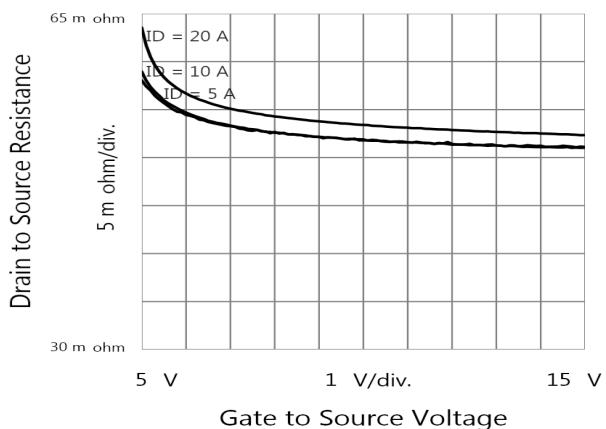
**Figure 1. Output Characteristics ( $T_J = 25^\circ\text{C}$ )**



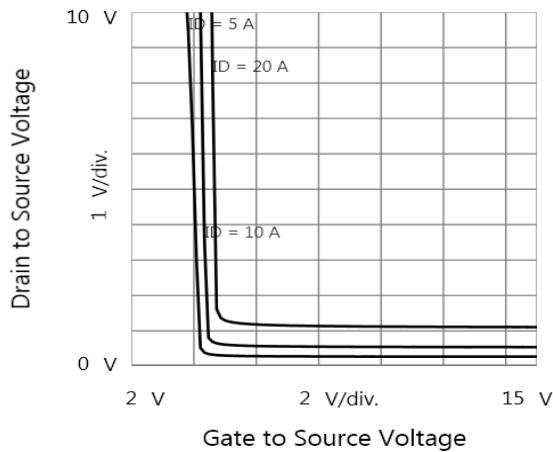
**Figure 2. Transfer Characteristics**



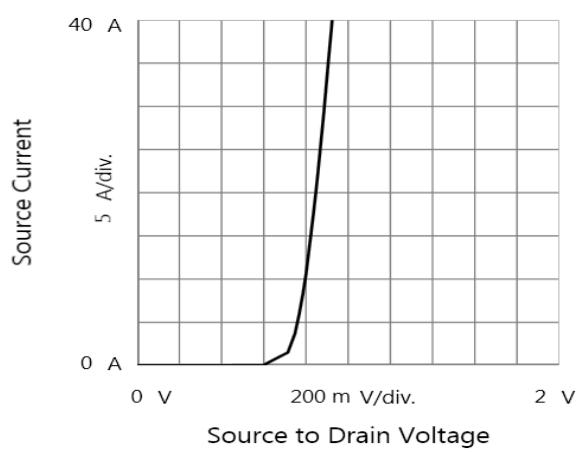
**Figure 3. Drain to Source Resistance vs. Drain Current**  $T^{\text{C}}$ , Case Temperature (A)



**Figure 4. Drain to Source Resistance vs. Gate to Source Voltage**  $T^{\text{C}}$ , Case Temperature ( $^\circ\text{C}$ )

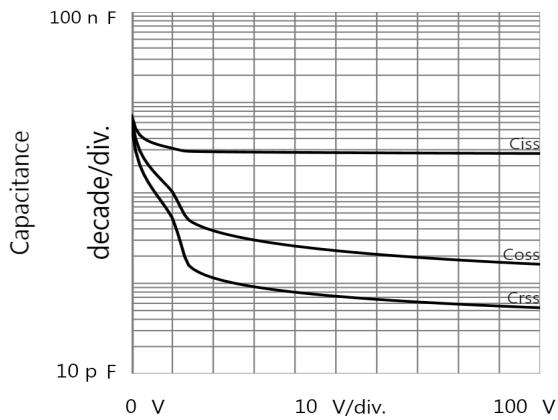


**Figure 5. Drain to Source Voltage vs. Gate to Source Voltage**

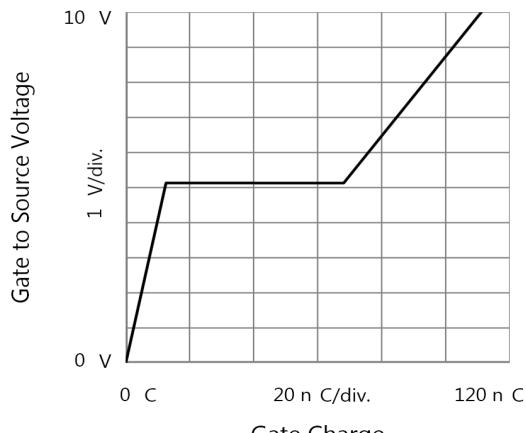


**Figure 6. Body Diode Forward Characteristics**

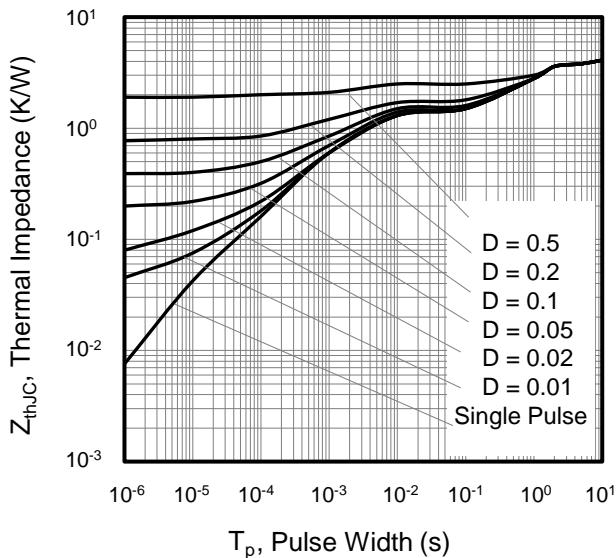
## 200V N-Channel Enhancement Mode MOSFET



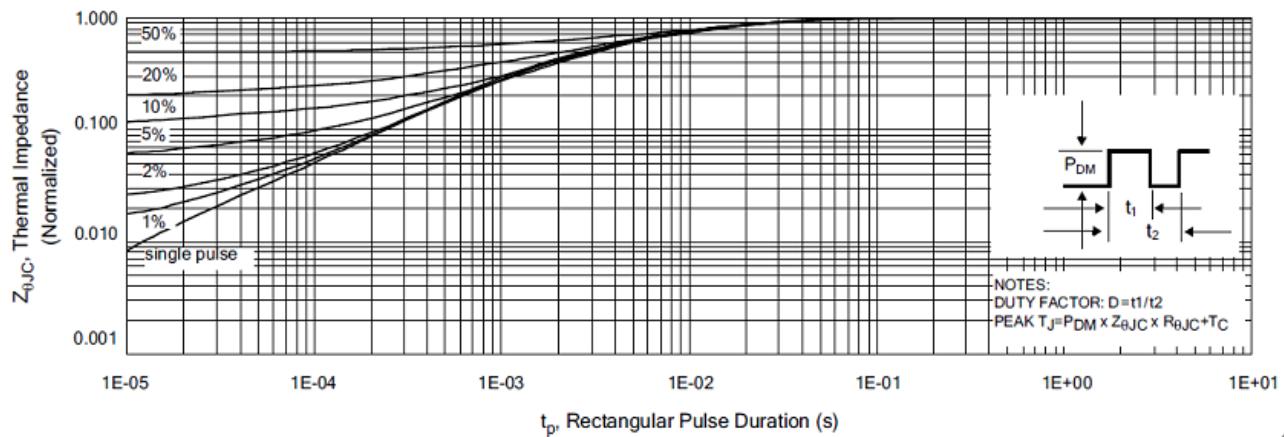
**Figure 7. Capacitance**



**Figure 8. Gate Charge**

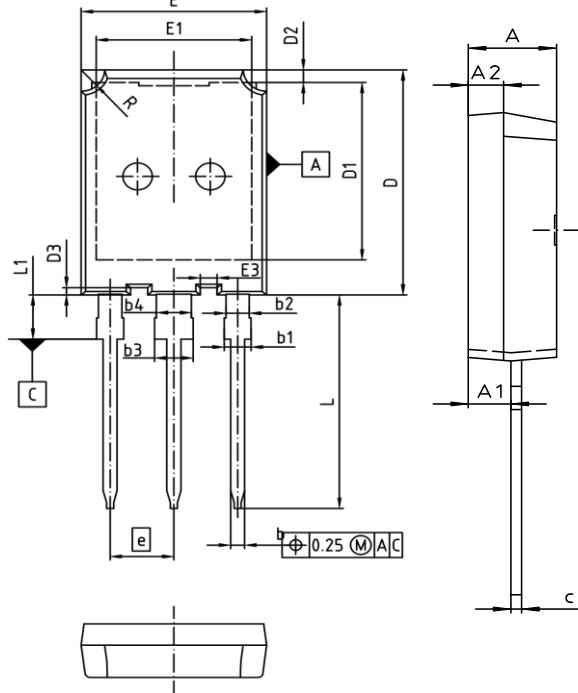


**Figure 11. Maximum Effective Thermal Impedance, Junction-to-Case**



## 200V N-Channel Enhancement Mode MOSFET

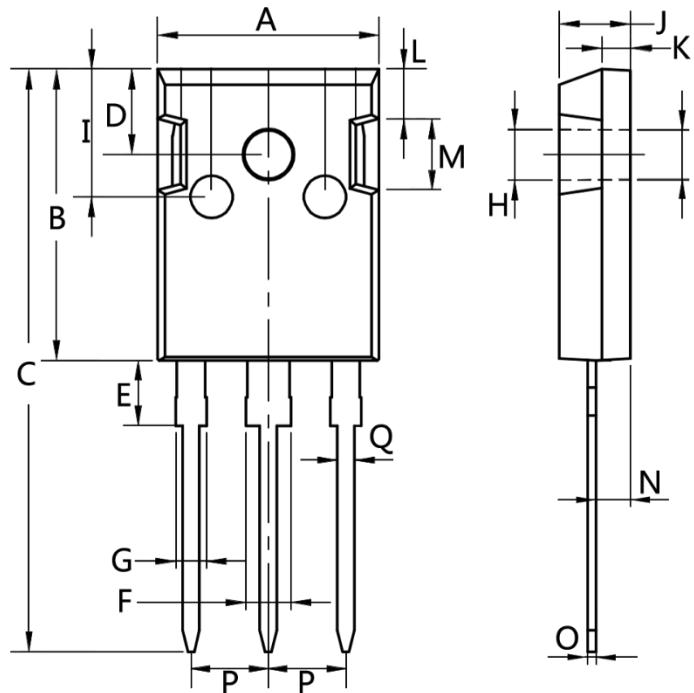
### Package Mechanical Data-TO-247-Plus-SLK



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.201
A1	2.31	2.51	0.091	0.099
A2	1.90	2.10	0.075	0.083
b	1.16	1.26	0.046	0.050
b1	1.96	2.25	0.077	0.089
b2	1.96	2.06	0.077	0.081
c	0.59	0.66	0.023	0.026
D	20.90	21.10	0.823	0.831
D1	16.25	16.85	0.640	0.663
D2	1.05	1.35	0.041	0.053
D3	0.58	0.78	0.023	0.031
E	15.70	15.90	0.618	0.626
E1	13.10	13.50	0.516	0.531
E3	1.35	1.55	0.053	0.061
e	5.44 (BSC)		0.214 (BSC)	
N	3		3	
L	19.80	20.10	0.780	0.791
L1	-	4.30	-	0.169
R	1.90	2.10	0.075	0.083

## 200V N-Channel Enhancement Mode MOSFET

### Package Mechanical Data-TO-247-LX



Dim.	Min.	Max.
A	15.0	16.0
B	20.0	21.0
C	41.0	42.0
D	5.0	6.0
E	4.0	5.0
F	2.5	3.5
G	1.75	2.5
H	3.0	3.5
I	8.0	10.0
J	4.9	5.1
K	1.9	2.1
L	3.5	4.0
M	4.75	5.25
N	2.0	3.0
O	0.55	0.75
P	Typ 5.08	
Q	1.2	1.3